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METHOD FOR MANUFACTURING A BIPOLAR INTEGRATED CIRCUIT USING I^2L

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Claim

Method for manufacturing a bipolar integrated circuit using I^2L characterized by the following facts: during the process for manufacturing bipolar integrated circuits using I^2L, which use emitters and collectors that operate in a reverse manner compared to conventional bipolar transistors, through the diffusion windows in the substrate of the integrated circuit, phosphorus or arsenic is diffused to form collector regions for the I^2L portion, and an insulating film is formed together with these regions; then, in the insulating film portion of said collector regions, contact holes smaller than said diffusion windows are formed; in the contact holes, a high-concentration polysilicon wiring for wiring of the I^2L circuit is formed and is connected to said collector regions; then, the second layer of metal wiring is applied.

Detailed explanation of the invention

This invention pertains to an improved method for manufacturing a bipolar integrated circuit using I^2L with a double-layer wiring configuration.

It is well known that this type of bipolar integrated circuit has inverters made of individual transistors with emitters and collectors that operate in a reverse manner with respect to conventional bipolar transistors, and transistors for complementary injection which have a common emitter and base and base and collector, respectively. However, compared with conventional bipolar integrated circuits, the current amplification rate (β_{up}) in the inverter is lower. Consequently, there is a demand for the improvement of the current amplification rate.

The conventional manufacturing process for bipolar integrated circuits using I^2L with double layer wiring is performed as follows. Conventional technology is used to form the first layer of aluminum wiring, and an interlayer insulating substance is deposited by CVD. Then, contact holes are formed in the film using photolithography. Then, a second layer of aluminum is formed by vapor deposition, followed by patterning to complete the circuit. However, in this method, after vapor deposition of the first and second aluminum layers, a high-temperature process (500°C or higher) cannot be carried out, and a cleaning step such as for phosphorus getter, etc., cannot be carried out. This is a problem. Also, the CVD film deposited as an insulating layer on the first layer of the aluminum reacts with aluminum, and electrical connection often cannot be guaranteed. This is also a problem.

In consideration of these problems, it has been proposed that the bipolar integrated circuit using I^2L be manufactured by forming the first layer of wiring from a high-concentration polysilicon instead of aluminum. For a conventional bipolar IC, polysilicon is used as a diffusion source, yet it has not been used as the wiring. That is, in this method, first of all, as shown in Figure 1a, on p^--type silicon substrate (1), n^+-type diffusion layer (2) is formed from Sb or As; then, n-type Si layer (3) is formed by means of epitaxial growth. Then, by means of boron

diffusion, p^+-separating region (4) is formed, followed by formation of n^+-diffusion region (5), injector and external base region (6), and real base region (7) by means of low-concentration boron diffusion. Then, silicon dioxide film (8) is set, and diffusion windows (9)...(9) are formed in this oxide film. Then, on silicon dioxide film (8), as the first layer of wiring material, phosphorus or arsenic-doped polysilicon film (10) is coated by a CVD method, and at the same time, phosphorus or arsenic is diffused through diffusion windows (9)...(9) to form collector regions (11)...(11) (see Figure 1b). Then, as shown in Figure 1c, by means of photolithography, polysilicon film (10) is etched to form the first layer of polysilicon wiring (10'). Then, phosphate silicate glass is coated to form insulating film (12) (see Figure 1d). Then, contact holes are formed in insulating film (12) and oxide film (8), and aluminum vapor deposition and selective etching are performed to form the second layer of wiring as ground portion (13), injector (14) and input portion (15). In this way, a bipolar integrated circuit using I^2L is formed (see Figure 1e).

However, in the aforementioned method, as polysilicon is directly coated on the oxide film having diffusion windows to form collector regions, as shown in Figure 2, the area of first layer wiring regions (10')...(10') made of polysilicon on collector regions (11)...(11) is larger than the area of collector regions (11)...(11). Also, it is necessary to maintain a prescribed width (usually 3 μm) between first layer wiring regions (10')...(10'). Consequently, the gap between collector regions (11)...(11) naturally becomes longer, the integration degree decreases significantly, the ratio of the area of the collector regions to the area of base regions (6) becomes smaller, and the current amplification rate (β_{up}) decreases. This is a disadvantage.

In order to solve the aforementioned problems, the inventors of this patent application performed extensive research. As a result of this research, it was found that by diffusing phosphorus or arsenic through the diffusion windows before forming the first layer wiring of polysilicon connected to the collector region and by forming an insulating film along with this diffusion process then by forming contact holes smaller than the diffusion windows in the insulating film and finally by forming the first layer wiring made of polysilicon, it is possible to form the first layer wiring on the collector regions in an area equal to or smaller than the area of the collector regions; so that the gap between the collector regions becomes smaller, the integration degree becomes higher, the ratio of the area of the collector regions to the area of the base regions becomes higher, the current amplification rate is improved significantly, and the bipolar integrated circuit using I^2L can perform high-speed operation. In this way, a method for manufacturing the device of the present invention was found.

That is, this invention provides a method for manufacturing a bipolar integrated circuit using I^2L characterized by the following facts: its emitter and collector operate in a reverse manner to conventional bipolar transistors, through the diffusion windows in the substrate of the

integrated circuit, phosphorus or arsenic is diffused to form collector regions for the I^2L portion, and an insulating film is formed together with these regions, then, in the insulating film portion of said collector regions, contact holes smaller than said diffusion windows are formed; in the contact holes, a high-concentration polysilicon wiring for wiring of the I^2L circuit is formed and is connected to said collector regions; then, the second layer of metal wiring is applied.

According to this invention, as means for forming the collector regions and for forming the insulating film, for example, the following methods may be used: a method in which phosphorus or arsenic ions are implanted through the diffusion windows followed by a thermal oxidation process to form an oxide film (insulating film); a method in which phosphate silicate glass or arsenate silicate glass is deposited by CVD through the diffusion windows, and by means of diffusion of phosphorus or arsenic, the collector regions and insulating film are formed at the same time, etc.

According to this invention, usually plural collector regions are formed.

In the following, this invention will be explained in more detail with reference to an application example illustrated by Figures 3a-f.

Application example

First of all, as shown in Figure 3a, on p^--type silicon substrate (21), n^+-diffusion layer (22) was formed by means of Sb, and then, by means of epitaxial growth, n-type Si layer (23) was formed. Then, by means of boron diffusion, p^+-separating region (24) was formed, followed by the formation of true base region (25), n^+-diffusion region (26), injector, and external base region (27) by means of low-concentration diffusion of boron. Then, by means of a thermal oxidation process, silicon dioxide film (28) was formed, and diffusion windows (29)...(29) were formed in oxide film (28). Then, as shown in Figure 3b, on the entire surface of silicon dioxide film (28), phosphate silicate glass film (30) (PSG film) with a thickness of 3000 Å was formed using the CVD method, and at the same time, phosphorus was made to diffuse from said PSG film (30) through diffusion windows (29)...(29) to form four collector regions (31)...(31) in true base region (25) and to form emitter region (32) in the n^+-diffusion layer.

Then, as shown in Figure 3c, on collector regions (31)...(31), contact holes (33)...(33) with an area smaller than said diffusion windows (29)...(29) were formed in portions of PSG film (30). In this case, contact hole (33') was also formed in the portion of PSG film (30) on emitter region (32). Then, a high-concentration polysilicon film was formed using the CVD method on PSG film (30) having contact holes (33)...(33), (33'), and by means of the conventional photolithographic method, patterning was performed to form first layer wiring regions (34)...(34) connected to said collector regions (31)...(31) and emitter regions (32) (see Figure 3d). Of course, it is also possible to diffuse phosphorus or As or the like in polysilicon after growth of

the undoped polysilicon by CVD method. Then, as shown in Figure 3e, on PSG film (30) containing first layer wiring regions (34)...(34), phosphate silicate glass film (35) (PSG film) with a thickness of 6000 Å was deposited. Then, wiring outlets (36), (36), (36) were formed on the portion of second layer PSG film (35) on wiring (34) of emitter region (32), the portion of oxide film (28) on injector region (27) and first and second PSG films (30), (35), and the portion of oxide film (28) on the external base and first and second PSG films (30), (35). Then, aluminum vapor deposition and selective etching were performed to form, as the second layer of wiring, ground portion (37), injector (38), and input portion (39). In this way, a bipolar integrated circuit using I^2L was obtained.

As shown in Figure 4, for the obtained integrated circuit, contact holes (33)...(33) smaller than diffusion windows (29)...(29) are formed in the PSG film in collector regions (31)...(31) in external base region (27). Through said contact holes (33)...(33), first layer wiring regions (34)...(34) are connected to said collector regions (31)...(31). That is, first layer wiring regions (34)...(34) have the same area as that of collector regions (31)...(31). Consequently, even when a prescribed width (about 3 μm) is maintained between first layer wiring regions (34)...(34), first layer wiring regions (34)...(34) are still aligned with collector regions (31)...(31). Consequently, one may separate collector regions (31)...(31) by a gap of only 3 μm, and the distance is much shorter than the distance between collector regions (31)...(31) in the conventional method (as shown in Figure 2). As a result, it is possible to increase the integration degree, and at the same time, it is possible to increase the ratio of the area of collector regions (31)...(31) to the area of external base region (27), and to improve the current amplification rate. Also, in this application example, when the diffusion windows have the same measurements as that in the conventional method, the integration degree is improved by 24% over that in the conventional method, and the current amplification rate is improved by 31% over that in the conventional method.

As explained in detail above, according to this invention, the first layer wiring regions formed on the collector regions of the I^2L portion can occupy equal or smaller area than the area of the collector regions, and the distance between the collector regions can be reduced so that the integration degree can be increased. Also, it is possible to increase the ratio of the area of the collector region to the area of the base region, so that it is possible to improve the current amplification rate significantly, so that the bipolar integrated circuit using I^2L can be used for high-speed operations.

Brief description of the figures

Figures 1a-e are cross-sectional views illustrating the manufacturing steps of the bipolar integrated circuit using I^2L in the prior art. Figure 2 is a plan view illustrating the base region of the integrated circuit obtained by the steps of operation described above. Figures 3a-f are

cross-sectional views illustrating the manufacturing steps of an integrated circuit using I^2L in this invention. Figure 4 is a plan view illustrating the base region of the integrated circuit obtained by the steps of operation shown in Figures 3a-f.

21 p^--type silicon substrate
27 External base region
28 Silicon dioxide film
29 Diffusion window
30 PSG film
31 Collector region
33 Contact hole
34 First layer wiring (Pol-Si)
37 Ground portion
38 Injector
39 Input portion

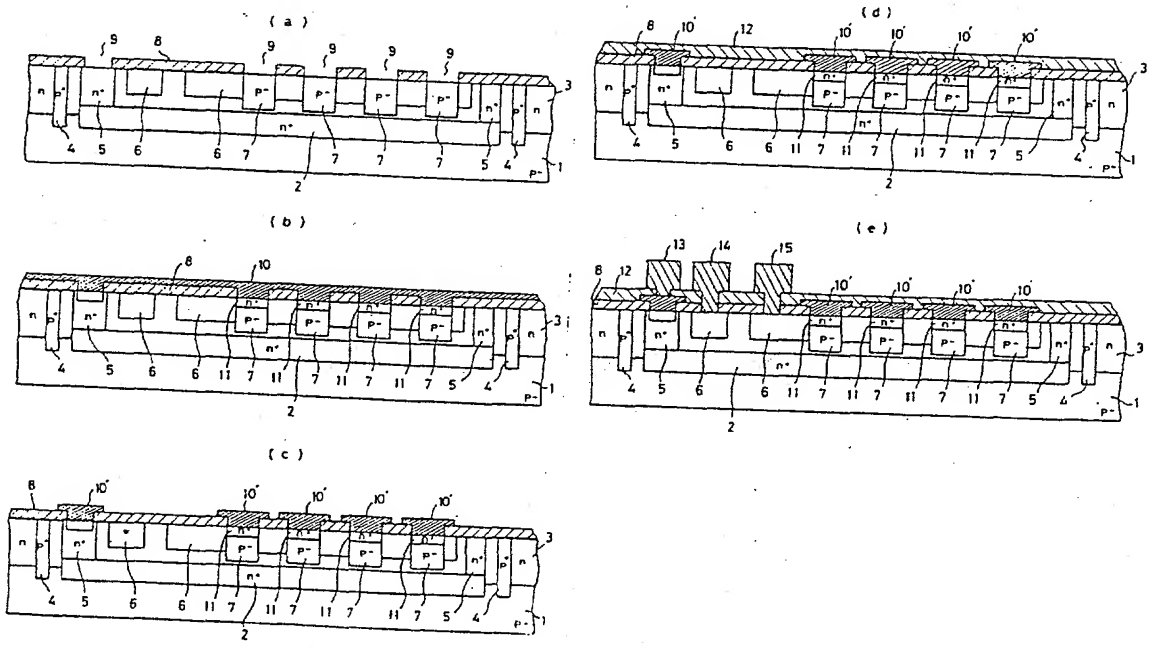

Figure 1

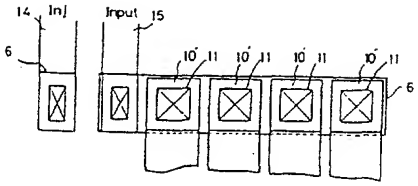

Figure 2

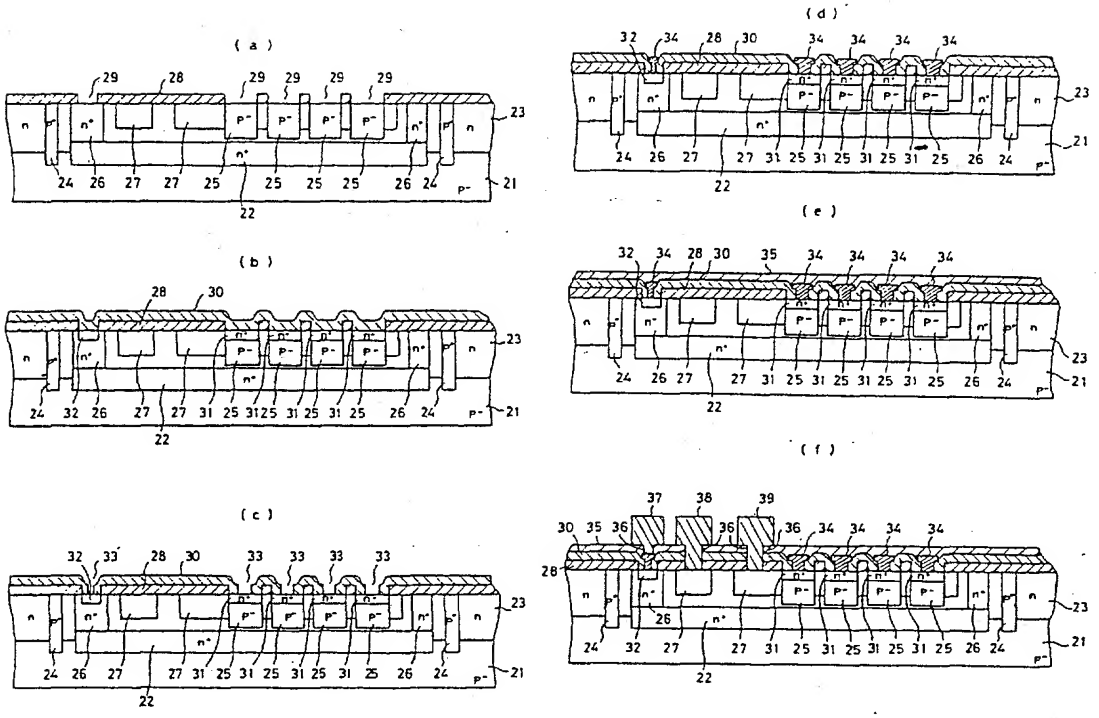

Figure 3

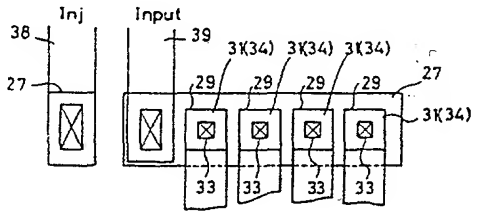

Figure 4

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

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（全 5 頁）

⑤4 I²Lを含むバイポーラ集積回路の製造方法

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⑦1特　願　昭53—82683

明　細　書

1.発明の名称

I²Lを含むバイポーラ集積回路の製造方法

2.特許請求の範囲

エミッタ，コレクタを通常のバイポーラトランジスタと逆動作するI²Lを含むバイポーラ集積回路の製造において、集積回路基体の拡散窓に、燐又は砒素を拡散してI²L部のコレクタ領域を形成するとともに絶縁膜を形成した後、前記コレクタ領域の絶縁膜部分に前記拡散窓より小さいコンタクトホールを設け、このコンタクトホールにI²L回路の配線のための高濃度多結晶シリコン配線を形成して前記コレクタ領域と接続させ、さらに第二層の金属配線を施すことを特徴とするI²Lを含むバイポーラ集積回路の製造方法。

3.発明の詳細な説明

本発明は二層配線構造をなすI²Lを含むバイポーラ集積回路の製造方法の改良に関する。

周知の如く、この種のバイポーラ集積回路はエミッタ，コレクタを通常のバイポーラトランジスタと逆にした逆動作バーティカルトランジスタからなるインバータと、そのエミッタ・ベースを夫々ベース，コレクタとして共有する相補型のインジェクタ用トランジスタとを備えたものであるが、通常のバイポーラ集積回路に比してインバータ中の電流増幅率（β_{up}）が低いために、電流増幅率を改善することが要望されている。

ところで、従来、I²Lを含む2層配線を行つたバイポーラ集積回路を製造するには次のようなことが行なわれている。即ち、周知の技術で一層アルミニウム配線を行ない、層間絶縁物をCVD膜で堆積させた後、この膜にコンタクトホールを写真蝕刻法により形成し、さらに第二層のアルミニウム蒸着及びパターンニングを行なつて完成する。しかしながら、この方法にあつては第一，第二のアルミニウム蒸着後の高温プロセス（500℃以上）が不可能であり、清浄化工程、例えばリンゲッター等が不可能となる問題

がある。また、第一層のアルミニウム上に絶縁体として堆積させるCVD膜と該アルミニウムとが反応して、しばしば電気接続が不可能となる問題がある。

このようなことから、以下に示す如く第一層配線をアルミニウムに代つて高濃度多結晶シリコンで形成してI^2Lを含むバイポーラ集積回路を製造することが考えられる。従来バイポーラICでは、多結晶Siは拡散源として使用されているが配線に使用されてはいない。即ち、まず第1図aに示すようにP型のシリコン基板1にSb又はAsでn^+拡散層2を、さらにエピタキシャル成長によりn型Si層3を形成した後、ボロン拡散によりp^+分離領域4を構成し、ひきつづきn^+拡散領域5、インジエクター及び外部ベース領域6、ボロンの低濃度拡散により真のベース領域7を形成し、さらにシリコン酸化膜8を設け、この酸化膜に拡散窓9…9を形成する。その後、シリコン酸化膜8上に第一層配線材料としてのリン或いはヒ素ドープ多結晶シリコン膜10をCVD法により被着すると共に拡散窓9…9からリン或いはヒ素を拡散してコレクタ領域11…11を形成する（第1図b図示）。つづいて第1図cに示すように写真蝕刻法により多結晶シリコン膜10をエッチングして第一層の多結晶シリコン配線10'を形成した後、リン珪化ガラス等を被着して絶縁膜12を形成する（第1図d図示）。次いで、絶縁膜12及び酸化膜8にコンタクトホールを明け、アルミニウム蒸着、選択エッチングを施して第二層配線としてのアース部13、インジエクター14、入力部15を構成し、I^2Lを含むバイポーラ集積回路を造る（第1図e図示）。

しかしながら、上記方法にあつては多結晶シリコンを拡散窓を有する酸化膜上に直接被着してコレクタ領域を形成するため第2図に示す如く、コレクタ領域11…11上の多結晶シリコンからなる第一層配線10'…10'がコレクタ領域11…11の面積より大きくなる。その上、第一層配線10'…10'間は所定の巾（通常3μm

は必要）を保持しなければならないため、コレクタ領域11…11の間隔が必然的に長くなり、集積度が著しく低下すると共にベース領域6の面積に対するコレクタ領域の面積の比が低くなり、電流増幅率（β_{up}）が低下する欠点がある。

これに対し、本発明者は上記欠点を解消するために鋭意研究を重ねた結果、コレクタ領域に接続させる多結晶シリコンの第一層配線を形成する際、予め拡散窓に燐又は砒素を拡散するとともに絶縁膜を形成し、この絶縁膜に拡散窓より小さいコンタクトホールを開口した後多結晶シリコンの第一層配線を形成することによつて、コレクタ領域上の第一層配線を該コレクタ領域の面積と同等乃至それより小さくでき、もつてコレクタ領域の間隔が短くなり集積度を向上できると共に、ベース領域面積に対するコレクタ領域面積の比が向上し電流増幅率を著しく改善でき、高速動作が可能なI^2Lを含むバイポーラ集積回路を製造し得る方法を見い出した。

すなわち、本発明方法はエミッタ，コレクタを通常のバイポーラトランジスタと逆にした構造のI^2Lを含むバイポーラ集積回路の製造において、集積回路基体の拡散窓に、燐又は砒素を拡散してI^2L部のコレクタ領域を形成するとともに絶縁膜を形成した後、前記コレクタ領域の絶縁膜部分に前記拡散窓より小さいコンタクトホールを設け、このコンタクトホールにI^2L回路の配線のための高濃度多結晶シリコン配線を形成して前記コレクタ領域と接続させ、さらに第二層の金属配線を施すことを特徴とするものである。

本発明におけるコレクタ領域の形成と絶縁膜の形成とを行なう手段としては、例えば拡散窓に燐又はヒ素をイオン注入した後熱酸化処理して酸化膜（絶縁膜）を形成する方法、或いは拡散窓に燐珪化ガラス又は砒素珪化ガラスをCVD法により被覆して該ガラスからの燐，砒素の拡散によりコレクタ領域と絶縁膜とを同時に形成する方法等が採用し得る。

本発明におけるコレクタ領域は通常複数個形

成されるものである。

次に、本発明の実施例を第3図a～fを参照して説明する。

実施例

まず第3図aに示すように、p^-形のシリコン基板21にSbでn^+拡散層22を、さらにエピタキシャル成長によりn型Si層23を形成した後、ボロン拡散によりp^+分離領域24を構成し、ひきつづきボロンの低濃度拡散により真のベース領域25、n^+拡散領域26、インジエクター及び外部ベース領域27を形成し、さらに熱酸化処理によりシリコン酸化膜28を設け、この酸化膜28に拡散窓29…29を形成した。その後、第3図bに示すようにシリコン酸化膜28全面に厚さ3000Åの燐珪化ガラス膜30（PSG膜）をCVD法により形成すると共に、該PSG膜30から燐を拡散窓29…29に拡散して真のベース領域25に4つのコレクタ領域31…31及びn^+拡散層にエミッタ領域32を形成した。

次いで、第3図cに示すように、コレクタ領域31…31上のPSG膜30部分に前記拡散窓29…29より小さい面積のコンタクトホール33…33をあけた。この場合、エミッタ領域32上のPSG膜30部分にもコンタクトホール33'をあけた。つづいて、コンタクトホール33…33，33'を有するPSG膜30上に高濃度多結晶シリコン膜をCVD法により被着し、通常の写真蝕刻法によりパターンニングして前記コレクタ領域31…31及びエミッタ領域32に接続した第一層の配線34…34を形成した（第3図d図示）。勿論、undope多結晶SiをCVD法で成長させた後、リン或いはAsを多結晶Siに拡散してもよい。その後、第3図eに示すように第一層の配線34…34を含むPSG膜30上に厚さ6000Åの燐珪化ガラス膜35（PSG膜）を被覆し、しかる後、エミッタ領域32の配線34上の第二層目のPSG膜35の部分、インジエクター領域27上の酸化膜28と第一，第二のPSG膜30，35との部分、及び外部ベース上の酸化膜28と第一，第二のPSG膜30，35との部分に配線取出口36，36，36をあけ、アルミニウム蒸着、選択エッチングを施して第二層配線としてのアース部37，インジエクター38，入力部39を構成し、I^2Lを含むバイポーラ集積回路を得た。

得られた集積回路は第4図に示すように外部ベース領域27内のコレクタ領域31…31上のPSG膜に拡散窓29…29より小さいコンタクトホール33…33が形成され、そのコンタクトホール33…33を介して第一層配線34…34が該コレクタ領域31…31と接続されている。つまり、第一層配線34…34がコレクタ領域31…31の面積と同等となる。このため、第一層配線34…34間を所定の巾（3μm程度）に保持してもその第一層配線34…34はコレクタ領域31…31と合致するので、コレクタ領域31…31を3μm離れればよくなり、実質的にコレクタ領域31…31間の距離を従来法（前述した第2図図示）に比して著しく短くなる。その結果、集積度を向上できると共に、外部ベース領域27の面積に対するコレクタ領域31…31の面積比が向上され、電流増幅率を改善できる。なお、本実施例において拡散窓を従来法と同寸法とした場合、集積度については従来法に比して24%程度改善され、かつ電流増幅率については従来法に比して31%改善されることがわかつた。

以上詳述した如く、本発明によればI^2L部のコレクタ領域上の第一層配線を、該コレクタ領域の面積と同等乃至それより小さくでき、もつてコレクタ領域の間隔を短くして集積度を向上できると共に、ベース領域の面積に対するコレクタ領域の面積比を向上して電流増幅率を著しく改善でき、高速動作が可能なI^2Lを含むバイポーラ集積回路を製造できる等顕著な効果を有する。

4.図面の簡単な説明

第1図a～eは従来のI^2Lを含むバイポーラ集積回路の製造工程を示す断面図、第2図は前記工程で得られた集積回路のベース領域を示す

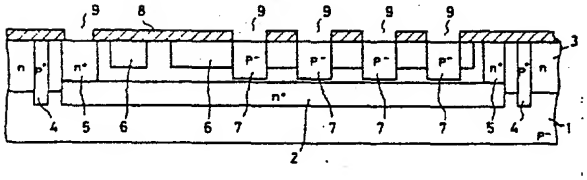
平面図、第3図a～fは本発明のI^2Lを含む集積回路の製造工程を示す断面図、第4図は前記第3図a～fの工程により得られた集積回路のベース領域を示す平面図である。

21…p⁻型シリコン基板、27…外部ベース領域、28…シリコン酸化膜、29…拡散窓、30…PSG膜、31…コレクタ領域、33…コンタクトホール、34…第一層配線（Pol-Si）、37…アース部、38…インジエクタ、39…入力部。

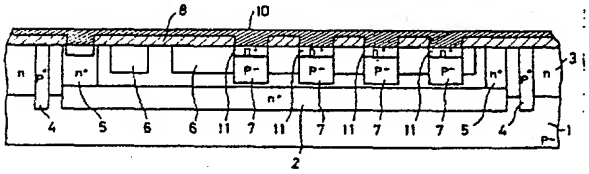
出願人代理人　弁理士　　鈴　江　武　彦

第1図

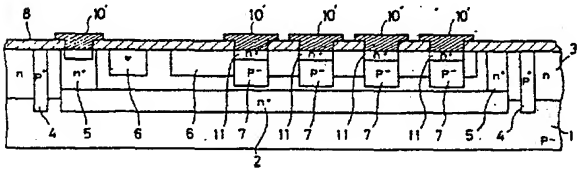
(a)



(b)

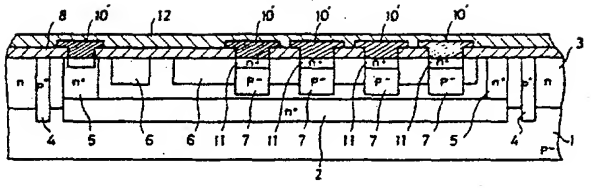


(c)

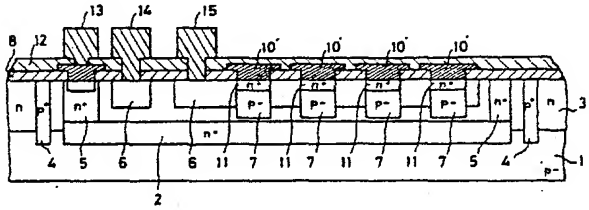


第1図

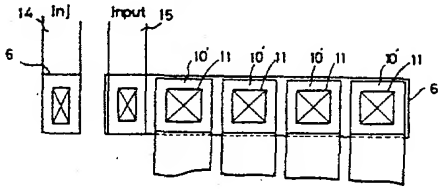
(d)



(e)

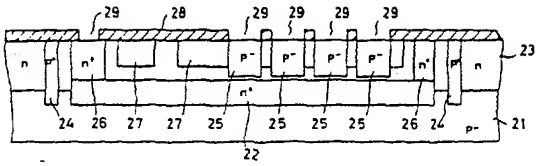


第2図

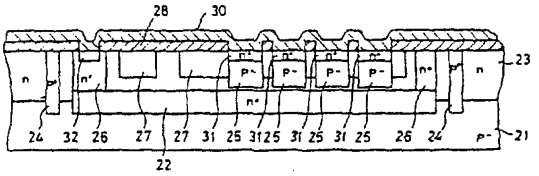


第 3 図

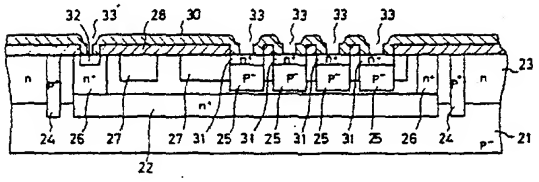
(a)



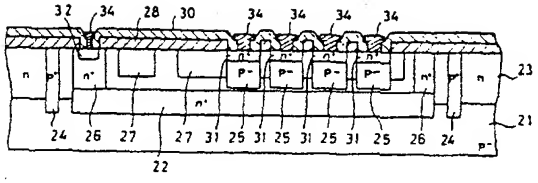
(b)



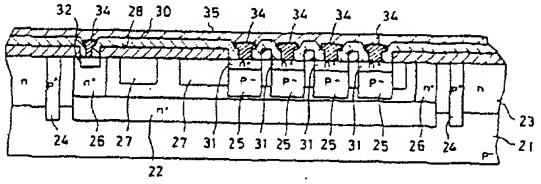
(c)



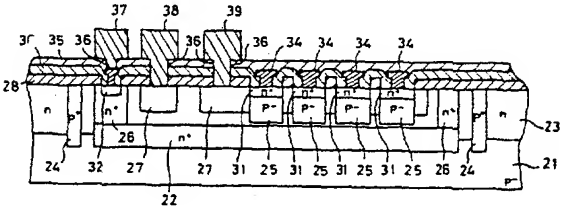
(d)



(e)



(f)



第 4 図